

Horizon 2020 European Union funding for Research & Innovation



# Facilitating Widespread Adoption of Edge Computing through development of a universal microserver architecture and software ecosystem



#### 1. Introduction

**UniServer** aims at creating smaller, energy efficient, resili-ent data centers closer to the users, that can preprocess the data and provide faster servicing of their data without the need to send all data to the cloud and wait for its response, in order to account for the capacity of the current Internet and cloud computing infrastructure becoming greatly satu-rated.

- HealthLog will exploit low-level hardware capabilities and will constantly monitor the status of the system and report any error appearance.
- Predictor will provide insight whether the system can operate under the applied system settings or the ones specified.
- StressLog will identify the limits of the system, in terms of operating margins for every system component.
- Hypervisor will synchronize and orchestrate all the above modules. In addition will provide recovery poli-cies in case of erratic behavior and will communicate with Openstack through customized LibVirt.







Uniserver combines *Edge/Fog Computing* and *intrinsic Heterogeneity* by shaving the rather conservative manufac-turer operation margins to a *just-right* point.

# 2. Challenges and Objectives

The main impediments towards making Big Data and IoT opportunities tangible have been identified and UniServer proposes to prevail over these challenges through its ob-jectives:

- Operate state-of-the-art computing platforms more ag-gressively.
- Trade off energy and performance gains.
- Develop novel technologies in various system layers to efficiently deal with potential faults that may occur.

• **Openstack** will orchestrate the VMs execution based on the characteristics of each workload and machine.

## 4. System hardware results





#### **DRAM Power Savings**

Reduce DRAM power usage by 23.2% on average without com-promising reliability or performance under relaxed voltage (5% less) and refresh rate (35 times).





#### **3.** System Software Stack



Illustration of the real-time execution of the UniServer demonstrator running Worldsensing DoSSensing Jammer Application.

Parameter	Nominal	UoA chip	UCY chip	QUB chip
Vmin – PMD	980 mV	930 mV	910 mV	930 mV
Vmin – SoC	950 mV	920 mV	870 mV	900 mV
Vmin – DRAM	1500 mV	1428 mV	1428 mV	1428 mV
Refresh Rate min – DRAM	64 ms	2279 ms	2279 ms	2279 ms
Total power savings		20.2%	12.5%	12.3%

There is a relatively **large variation of voltage guardband among the chips**.





## **5.** System software results

Improved kernel resilience through migration of fault-sensitive code execution to reliable cores



Refresh interval reduced to 2.28s and voltage reduced to 1.43V. Every 10°C increase leads to an order of magnitude increase in the number of unique weak cells.

This approach eliminates freezes/crashes and increases observ-ability of errors that can now be used as an <u>early</u> warning be-fore a crash, up to 10sec in advance.

The research leading to these results has received funding from the European Community through the H2020 programme for research and technical development, grant agreement no. 688540 Project Info: http://www.uniserver2020.eu/ | Contact: uniserver-info@qub.ac.uk , Coordinator: Georgios Karakonstantis | www.facebook.com/uniserver2020/ https:/twitter.com/uniservereu | https://www.youtube.com/channel/UCxCT4ge4t-5oWpay8Gyp\_YQ | https://www.linkedin.com/company/uniserver/